‘Golden’ timing signoff – does it correlate to Spice?

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“Whoever has the gold makes the rules” is certainly true in the world of signoff timing analysis. As more and more semiconductor companies converge to the same “golden” tool standard, it is important to understand the possible risks and dangers to future IC designs.

At my former company, we spent an inordinate amount of time qualifying delay calculation tools. As an ASIC vendor, we were ultimately responsible for guaranteeing that timing results matched silicon. The generation of “right first time silicon” was a mantra that was religiously recited internally and was a key element of winning business.

In the early days, like many of our competitors, we relied upon our own home-brewed physical design and timing analysis tools. Complete control over design flow, analysis and fabrication was a major benefit of our investment. Test chips were used to refine Spice models, and Spice was used to refine our delay calculation engines. The end result was a supreme confidence that chips would work coming out of the fab through the convergence of models and tools to a Spice standard.

While big companies were able to dedicate the resources to writing their own tools, smaller companies began to rely upon the EDA industry to do if for them, and it fell to EDA vendors to perform “due diligence” on matters of correlation. EDA companies took on the task of qualifying their tools with the help of customers, and soon designs began taping out with considerable success.

Many of the issues and effects that we see today -- crosstalk, slew degradation, on chip variation (OCV) -- were largely ignored since process technology had not progressed into the realm of deep submicron. The end result was a continued reliance on the EDA vendor to do the right thing, and a strengthening confidence in the tools based on working silicon. It sounds reasonable to say that “the tools are great because my silicon isn’t failing,” but let’s step back and take a closer look.

The generally accepted practice over the last several years has been to perform corner signoff for process, voltage, and temperature. If we assume a 3-sigma variation for each component, then you have a signoff point that is much more extreme than 3-sigma under actual worst-case conditions (see Figure 1). Naturally, almost every part produced is going to work as long as your delay calculator is marginally good enough due to this huge guardband.

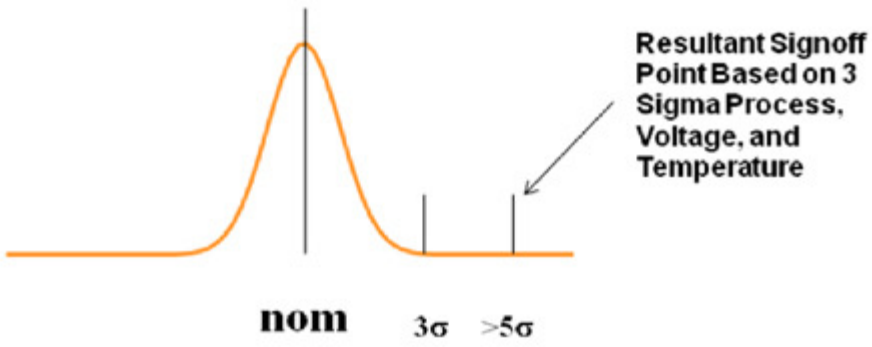

Figure 1 – Corner signoff based on 3-sigma PVT

But what if parts manufactured in the worst-case process *do* operate at the worst-case conditions? If you have the luxury of getting skewed parts and running tests at extreme environmental conditions, then you can get a general idea of how well your timing analysis matches silicon. But what if you can't?

Correlation loses vigilance

Back in the recent past, cost cutting and growing R&D expenses have pushed even the biggest companies to throw in the towel on internal IC layout and timing analysis solutions. Many of these companies have started to build a track record of working silicon with the most popular timing analysis tool vendors.

For most companies with a few years of successful tapeouts, the vigilance of correlation to Spice has been replaced with a simple test of obtaining consistent results from release to release. Only the companies with resources to burn can continue to qualify every release of the tools with respect to Spice on new technologies and for analysis of signal integrity (SI) effects. As timing for complex IP blocks is closed with third party tools, users are left in a precarious situation should they decide to do their own "due diligence" and benchmark the tools themselves.

What would happen if they suddenly discovered that they have fabricated designs that now result in timing violations when measured against Spice? The pragmatic approach would be to ignore these violations,since the designs are already working in silicon. But what ASIC vendor or IDM would want to go to sleep at night knowing that their design might not work at real life conditions?

When a new timing tool is introduced to a user, the predominant question asked by the user is not "How does it correlate to Spice?" but "How does it correlate to my incumbent tool?" The fixation on correlation to incumbent tools is understandable from a legacy standpoint. But it is puzzling when you consider that this comes from engineers, the last people I would expect to bury their heads in the sand. Engineers are inherently detail

oriented and focused on finding right answers. But these basic characteristics are too often shelved, so long as chips work as designed.

The lack of due diligence by methodology/CAD engineers is resulting in a dangerous drift towards signoff standards built upon illusory correlations instead of reality. This paradigm has moved some EDA vendors to go so far as to purposely dumb down their tools to match the results of a customer's existing tool, all done in the pursuit of trying to win the customer.

A string of successful tapeouts does not alone prove the accuracy or usefulness of a tool. It only serves to prove that the summation of the actual production process, coupled with environmental conditions and tool and modeling errors, were not sufficient to exceed the worst case conditions simulated.

Customers need to take a vested interest in ensuring that timing correlation is built upon a data-driven methodology that is confined to as few variables as possible. They need to step back and reassess where their existing tools stand with respect to Spice-level standards before they move on to 45 nm and 32 nm designs where SI and OCV concerns become even more dominant. Resource shortages at IDMs may tempt customers to take the easy road, but too many things have changed since the days of 180 and 130 nm to rely upon historical results to trust the tools for your next tapeout.

During Spice-based qualification of one of the more popular signoff tools, we found that the mean timing of test structures to be on the optimistic side. The point is regardless of the history or reputation of an EDA vendor, engineers need to maintain a data-driven approach to qualification in order to keep vendors honest and continue innovation.

Most users realize the fallacy of a legacy based correlation approach, but with each IP block that is signed off and with each design tapeout, they become more dependent on the vendor to perform the Spice-level correlation work. Despite this they continue to equate a legacy tool with a golden standard, creating an environment where legacy tool shortcomings define a standard. The end result stunts the innovation of new tool providers due to conformance issues, adds unknown risk to design success, and disregards the reality of what a timing violation is.

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