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Orora Unveils Automated Analog Behavioral Model Generation with 100x-1000x Speedup over SPICE for Complex Mixed-Signal Verification

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REDMOND, Wash.--(BUSINESS WIRE)--Orora Design Technologies, Inc., a company focused on automating mixed-signal IC design and verification, today unveiled Arana behavioral modeling platform. Arana is the industry's first tool to automatically extract *intelligent* behavioral models in Verilog-A/MS/D from a circuit netlist, offering 100x to 1000x speedup for complex mixed-signal functional verification.

Arana is the culmination of ten years of innovative research at Orora supported by the Defense Advanced Research Projects Agency, Defense Threat Reduction Agency, and Air Force Research Laboratory. Over twenty semiconductor companies have validated Arana on forty production circuits including phase-locked loops, data converters, SerDes, DC-DC converters, memory, and custom-digital circuits.

"As a leading design house for high-performance defense and space electronics, we started to use Orora's tools in 2003," said Dr. Warren Snapp, director of Boeing's Phantom Work, Solid State Electronics Development. "Arana is the only tool that allows us to verify our 90nm radiation-hardened XAUI SerDes design. For a SerDes transmitter driver, Arana speeds up SPICE by 1200 times. With Arana behavioral models, we discovered several design errors that would otherwise have gone to fabrication."

"Behavioral modeling has been regarded as a strategic yet most difficult-to-use technology for mixed-signal design," according to Dr. Prasad Subramaniam, vice president of Design Technology, eSilicon Corporation. "Many groups adopting behavioral modeling have invested in manually creating behavioral models. Unfortunately, quality modeling engineers are hard to find. Furthermore, it is difficult to maintain consistency between models and circuits. This is especially an issue for complex mixed-signal designs where analog circuits utilize extensive digital control, and have frequent specification changes up to the last minute," added Dr. Subramaniam. "With Arana, a designer without expert knowledge of behavioral modeling languages can quickly generate models consistent with his or her circuit design."

For design verification, Arana offers three dramatic advantages that cannot be matched by any fast SPICE simulator. (1) Efficiency: Automatically extracted pin-compatible behavioral models faithfully represent silicon and are 100x to 1000x faster than SPICE. (2) Intelligence: In case of a design error, a SPICE simulator will not offer much insight. In contrast, intelligent behavioral models can rapidly help to pinpoint design and integration errors, enabling silicon debugging. (3) Compatibility with well-established digital verification methodologies: Formal analog assertions are automatically generated to account for circuit operational and interface constraints.

Existing behavioral model generation tools are based on developing test benches and then "pre-storing" the results from test bench simulation in lookup tables, or using test benches to calibrate existing model templates. Both require intensive test bench and template construction and have limited application.

"In contrast, Arana is based on formulating circuit equations in the same way as any SPICE simulator, and then applying the rigorous theory of model abstraction," noted Dr. Richard Shi, the Arana architect. An elected fellow of IEEE, Dr. Shi participated in the creation of IEEE analog and mixed-signal (AMS) language industry standards, and has been recognized with the prestigious IEEE Donald O. Pederson Best Paper Award for his research on model order reduction.

"Verification often amounts to over half of the total chip design cost," added Dr. Shi. "Since most failures causing mixed-signal chip re-spins are due to simple connectivity and logic errors at the analog and digital interface, Arana provides an enabler for simulation-based mixed-signal function verification."

In addition to behavioral model generation from a netlist, Arana facilitates the creation of behavioral models as part of the top-

down design process. Arana supports a comprehensive behavioral modeling methodology including model optimization, validation, test bench generation, and reuse. Arana has been tightly integrated in Cadence Virtuoso Analog Design Environment, and can run standalone with any pre-layout or post-layout netlist as the input.

Price and Availability

Arana is now available pricing begins at $88,000 for a one-year time-based license.

Orora at DAC 2009

Orora will feature Arana behavioral modeling platform and Arsyn automated design platform at DAC, Booth 4151. For more information or to register for a product demo, visit www.orora.com.

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